This parallel interface diagnostic is one designed to locate problems in the SWTPC 6800 Computer System parallel interface board, MP-L. It is assumed that before loading this program the rest of the system is functioning normally with no problems. The program itself uses 33₁₀ words and is loaded within the 128 word RAM used by the MIKBUG operating system on the MP-A Microprocessor/ System Board. A program may reside in external RAM memory simultaneously with the diagnostic loaded within the 128 word RAM, or the diagnostic may be run with no MP-M memory boards installed on the system at all. The diagnostic may be loaded either from tape or instruction by instruction using MIKBUG starting from address A048, thru A068. The address of the parallel interface to be diagnosed is set by using MIKBUG to load the hexadecimal address of the selected port into memory locations A002 and A003 with the most significant byte going into A002 and the least significant byte going into A003. The starting address locations of the interface ports are given below:

Port	Address in Hex
I/O #0	8000
I/O #1	8004 (reserved for control interface)
I/O #2	8008
I/O #3	800C
I/O #4	8010
I/O #5	8014
I/O #6	8018
I/O #7	801C

Since the program counter is set when the program is initially loaded, the diagnostic is initiated as described in the "Go to User's Program" section of the Engineering Note 100. Once initiated, the program can be stopped only by depressing the "RESET" button. The program may then be re-started after resetting the program counter to A04A as described in the "Display contents of MPU Registers Function" section of Engineering Note 100.

The diagnostic itself works by echoing everything entered from the control terminal's keyboard back to the control terminal's display thru the parallel interface board. The control terminal remains connected to the serial control interface (I/O port A). The normal "echo" of the control interface is first software disabled and data is then transferred thru hardwired jumpers from the parallel interface's input to output ports. Neither interrupts nor the CA, CA2, CB1 or CB2 lines are tested. It is unlikely that the rest of the interface would check properly with only these lines inoperative.

To check the board, first make the following jumper connections on the MP-L parallel interface board I/O male connectors:

INPUT CONNECTOR		OUTPUT	CONNECTOR
IO	to	·	00
Il	to		01
12	to		02
13	to		03
14	to		04
15	to		05
16	to		06
17	to		07

Plug the wired connectors onto their positions on the MP-L interface board and with the power off, plug the board onto the selected interface location. Power up the system and load in the diagnostic program and the address of the parallel interface. Then execute a "Go to User's Program" as described in Engineering Note 100. Now as each character is typed, it will be "echoed" back and printed on the control terminal's display. At low control interface baud rates you will notice a delay in the "echo" function which is due to the software "echo" routine. You may also notice that the "echo" doesn't work properly if you type too fast. This is normal.

If you have problems, check the data on the output connector of the interface after each key is struck. Bits 0 thru 6 on the connector should be identical to the ASCII bit pattern of the key struck with bit 7 always a zero. The data should remain latched on the output of the interface until the next key is struck.

Never install or remove the interface board when the system is powered up. Doing so is not only hazardous to the equipment, but bypasses the normal powerup sequence required by the internal registers within the 6820 integrated circuit in order to guarantee proper operation.

SWTPC Parallel Interface Diagnostic PARTINT-1

A002 A003 E1AC E1D1			MSB OF PARADR (PIA address) LSB OF PARADR (PIA address) SUBROUTINE INEEE SUBROUTINE OUTEEE
			Start Loading Program At A04A
A048	A0		(Program Counter MSB)
A049	4A		(Program Counter LSB)
A04A	86	START	LDA A #\$3A
A04B	3C		
A04C	в7		STA A #\$8007
A04D	80		
A04E	07		
A04F	FE		LDX PARADR
A05B	A0		
A051	02		TD3 D 400
A052	C6		IDA B #\$FF
A053	FF		CTA D O V
A054 A055	E7 00		STA B 0,X
A055 A056	53		COM B
A050 A057	53 E7		STA B 2,X
A058	02		DIA D Z,A
A059	A7		STA A 1,X
A05A	01		211 11 1,11
A05B	A7		STA A 3,X
A05C	03		·
A05D	BD	LOOP1	JSR INEEE
A05E	E1		
A05F	AC		
A060	A7		0,X
A061	00		
A062	Аб		LDA A 2,X
A063	02		
A064	BD		JSR OUTEEE
A065	E1		
A066	Dl		DD 1 100D1
A067	20		BRA LOOP1
A068	F4		END
			END