ECONORAM VII A
USER'S MANUAL

24K x 8 static memory • S-100
using MM5257/TMS40144 • 4MHz
ABOUT ECONORAM VII

Congratulations on your decision to purchase ECONORAM VII, a 24K x 8 memory board designed specifically for electrical and mechanical compatibility with the S-100 bus standard. The S-100 bus is one of the most popular in the industry and by far the most prolific; we believe this board, with the rest of the S-100 portion of the ECONORAM family, is one of the best memory boards available for that bus.

We recommend that the parts in this kit be checked against the parts list for completeness and that these instructions be read through carefully before starting. Completion of the assembly should take from one to four hours, depending on previous assembly experience, and upon completion, you will discover -- as thousands of satisfied ECONORAM owners have discovered -- the pleasure of using a fine memory board that just works, and works, and works.

As the first company to nationally offer memory kits to computer hobbyists, we again thank you for choosing ECONORAM VII...welcome to the club.

TECHNICAL OVERVIEW

This board incorporates proven static memory technology. There are currently two popular types of memory being used in products such as this: static and dynamic. Static memories are the overwhelming choice in applications where speed, complexity, ease of use, and reliability must all be considered. There is no refresh slowdown, the CPU is freed from the drudgery of caretaking the memory, and techniques such as direct memory access (DMA) are far more reliable and easier to implement.

The individual memory ICs used on this board are grouped together to form four larger blocks of memory, two 4K x 8s and two 8K x 8s. The 8K blocks may be addressed on any 4K boundary, and the 8K blocks on any 8K boundary by setting the starting locations with the on-board dip switch (no jumpers required). Additional features include write protect switches for each of the four blocks; a write strobe selection switch which allows use of memory in systems, with or without a front panel (MWRITE strobe); allowance for use with or without the PHANTOM line; thorough capacitor bypassing of supply lines to suppress transients plus on-board regulation and heat-sinking for reliably cool operation. All this and sockets for all ICs go onto a double-sided, solder-masked printed circuit board with a complete component-layout legend.

Parts List

Upon receipt of your kit, check your parts against the list below.

☐ (1) Econoram VIIa circuit board

INTEGRATED CIRCUITS (note: the following parts may have letter suffixes and prefixes along with the key numbers given below)

☐ (48) MM5257N-3L or TMS 40L44 (U14 - U61)
☐ (1) 74LS00 nand gate (U5)
☐ (1) 74LS10 3-input nand gate (U7)
☐ (1) 74LS02 nor gate (U6)
☐ (5) 74S304 hex inverters (U8 - U12)
☐ (1) 74LS240 TRI-STATE inverters (U13)
☐ (4) 74LS266 ex-nor in.c. (U1 - U4)
☐ (4) 7805 positive 5V regulators (U62 - U65)

OTHER ELECTRONIC COMPONENTS

☐ (3) S.P. resistor packs (R1 - R3)*
☐ (3) 2.7K 1/4 watt resistors (red-violet-red; R4 - R6)
☐ (3) 39UF tantalum capacitors (C1 - C8)
☐ (25) ceramic disk bypass capacitors*

MECHANICAL COMPONENTS

☐ (61) low profile sockets*
☐ (3) dipswitch (S1 - S3)*
☐ (4) TO-220 heat sinks
☐ (4) 6-32 bolts
☐ (4) 6-32 lockwashers
☐ (4) 6-32 hex nuts
☐ (1) instruction booklet

*supplied already soldered to board.
MEMORY ADDRESS CONFIGURATION

This board is configured as two 4K blocks addressable on 4K boundaries and two 8K blocks independently addressable on 8K boundaries. Switches S1 and S2 each select one 4K and one 8K block. (Switch S1: block A - 4K and block B - 8K; switch S2: block C - 4K and block D - 8K) as follows:

<table>
<thead>
<tr>
<th>4K</th>
<th>SWITCH STARTING ADDRESS</th>
<th>8K</th>
<th>SWITCH STARTING ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2 3 4</td>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>0000H</td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>0000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>0000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>0000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 4000H</td>
<td>g1 g2 g3 g4</td>
<td>1000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 5000H</td>
<td>g1 g2 g3 g4</td>
<td>2000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>1111H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 4000H</td>
<td>g1 g2 g3 g4</td>
<td>3000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 5000H</td>
<td>g1 g2 g3 g4</td>
<td>4000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>5000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 4000H</td>
<td>g1 g2 g3 g4</td>
<td>6000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 5000H</td>
<td>g1 g2 g3 g4</td>
<td>7000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>8000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 4000H</td>
<td>g1 g2 g3 g4</td>
<td>9000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 5000H</td>
<td>g1 g2 g3 g4</td>
<td>A000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>B000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 4000H</td>
<td>g1 g2 g3 g4</td>
<td>C000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 5000H</td>
<td>g1 g2 g3 g4</td>
<td>D000H</td>
<td></td>
</tr>
<tr>
<td>g1 g2 g3 g4 3000H</td>
<td>g1 g2 g3 g4</td>
<td>E000H</td>
<td></td>
</tr>
</tbody>
</table>

In addition, position 8 on each switch enables (OFF) or disables (ON) the associated 8K block. Positions 1 and 2 of switch S3 disable/enable the 4K blocks A and C respectively.

MEMORY PROTECT SWITCHES

Switch S3 positions 3-6 are write enable switches. Converting them may be used for manual write protection of the memory. Each position 3, 4, 5 and 6 is associated with one memory block. A, B, C and D respectively. Any combination of these four switches may be ON write enable or OFF write protecting the particular block.

WRITE STROBE SELECT SWITCHES

Switch S3 positions 7 and 8 select write strobe. S3-7 ON causes PWR to qualify the memory for write commands. S3-7 ON causes MWRITE to qualify the memory for write commands. In normal operations with systems which have front panels ie., kitlab, instal etc., or others which generate MWRITE with or without front panels use MWRITE. All others use PWR. Positions 7 and 8 both ON at the same time will ground MWRITE on the bus. This condition must be avoided if MWRITE is present.

MEMORY TESTING

If the memory board seems to be working properly, the Memory Testing Routine (page 11) can be used to give the board a more thorough workout. It is rather slow; but will do the job well it can be entered via editor/assembly or front panel switch.

The routine is set up to test 24K, from 0000 hex up to AFFFF hex. This may be changed by entering a different starting address at "STRT" (3001 - 3002) and/or a different end address at "END" (3004 - high order byte only).

If the memory passes the test it starts over again. You may on the other hand, insert a jump instruction at "MARK" to some user routine or, if desired the user may enter an output instruction or, can do a notification routine at "MARK" to show successful completion and restart.

If the memory fails the test, critical information is stored and the routine enters a software "HALT", that is a jump here at "SHLT". Front panel lights, if any, will show this state. The user may then use the front panel or jump routines to display the following stored fault info:

- 3009H "FDE" = D, E pair... D is the fill character and E is the test character
- 3008H "FML" = H, L pair... the failure address
- 30EDH "FOUT" = the data expected at this address
- 30E6H "FIN" = the data read from the address
- * address from Memory Testing Routine Listing

The user may replace the "jump" at "SHLT" with a jump to a display or notification routine.

The difference between "FOUT" and "FIN" should indicate which bit is failing, indicating which chip or area is causing the problem.

This test will find most of the harder to distinguish errors.

PHANTOM LINE

In response to increasing numbers of users who have requested inclusion of PHANTOM LINE, bus pin 67 which is often used for implementing power on jump features. This board is designed for use with active or inactive PHANTOM lines.

CAUTION

Some manufacturers use PHANTOM line (bus pin 67) for a refresh signal. This will conflict with the PHANTOM feature, and cause boards with PHANTOM to fail. If your system has this conflict it must be resolved by either eliminating the refresh signal on the CPU board or disabling the PHANTOM feature on this and other boards.

The PHANTOM feature may be disabled by cutting the trace on the back of the PC board between pads for J1. It may be reactivated at any time simply by installing a jumper at J1 (see Figure 11).

If you want the PHANTOM feature, the conflicting refresh signal may be eliminated (IF NOT USED-SEE WHERE IN THE SYSTEM) by cutting the trace connected to bus pin 67 on the CPU board. BE SURE OF YOUR SYSTEM CONFIGURATION BEFORE CUTTING ANY TRACES.

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CIRCUIT DESCRIPTION

The heart of Econorm VII is the MMS257/TMS4044 static memory IC (RAM), which can store 4096 single bits of information (thus, each is a "4k x 1" memory IC). Unlike standard RAMs, those included with your kit are specifically designated by the manufacturer as low power, high speed parts.

These ICs are arranged in rows that are 8 ICs wide. This way, each row can store 4k x 8 bits of information. Paralleling 6 of these rows together produces a total memory storage of 24k x 8 bits. (Note that the bit number corresponding to a given column of ICs is indicated along the top edge of the memory array).

Now that we have this storage, there are still other aspects we must consider. First, we need to address a specific location in memory; and, we need to be able to write data into the memory, or read data from the memory.

The schematics on pages 8 and 9 show the address circuitry along with the other Econorm VII circuitry. Each memory IC requires 12 address bits (AD0-A11) to access any one of the 4096 bits available in the IC. These address bits are generated by the CPU and are buffered by a number of inverters. After buffering, a particular address is presented to all IC address selection pins. However, we additionally need to select which particular row of ICs is to be read to the given address. This requires 4 more address bits (A12-A15), which are decoded and used to enable the desired row of ICs (note row markings along the right hand side of the memory array).

When data is to be written into memory, it first passes through 0 inverters driving 0 buffers before being put on the data pins of the RAMs (buffering prevents loading of the data buses). Data to be read on to the data buses from memory passes through 8 transistor inverters driving 0 buffers; when data is not being read on to the bus, the outputs of these inverters are in a high-impedance or "disconnected" state.

An unfortunate fact of life is that logic ICs generate switching transients that travel along the power supply lines. If these transients work their way into the logic circuitry, problems can appear. To prevent such occurrences, bypass capacitors are tied across the power lines at regular intervals to filter the transients and allow them to be dissipated at every support point.

This board is guaranteed to operate at 4.5 volts over the full temperature range (0° - 70°C ambient) and to draw less than 2500 mA (2.5 amps). Our typical measured currents were less than 1210 mA at cold start-up, rapidly decreasing to around 1600-1900 mA, depending on the surrounding temperature. We have heard similar reports from the people already using these boards.

It is interesting to note that while static RAM technology has progressed to the point that this high-performance static RAM board is comparable in cost and power consumption to dynamic memory boards.

THANK YOU

This board is the result of much time, work and experience on the part of a number of people.

We strive for a board that doesn't just work the first time, but continues to give reliable operation for a long time. If we can be of any help to you in applying this board, or if you have any questions, please let us know. As always, we solicit your comments, letters, and new product suggestions.

HAPPY COMPUTING!